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10/816,311	03/31/2004	Nick Lindert	42P18257	9112

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EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,311	LINDERT ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 43-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *43* is/are allowed.

6)☒ Claim(s) *1-10,12-19 and 44-51* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/13/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Regarding claim 45, it is not clear what a specific material (i.e. SiGe, SiC...) is being used to form the semiconductor body that has a lattice constant larger than that of the bulk semiconductor substrate. Nowhere is this material recited in the disclosure. Without recitation of this material, one of ordinary skill in the art cannot ascertain how this feature can be achieved.

Regarding claim 46, it is not clear what a specific material (i.e. SiGe, SiC...) is being used to form the semiconductor body that has a lattice constant smaller than that of the bulk semiconductor substrate. Nowhere is this material recited in the disclosure. Without recitation of this material, one of ordinary skill in the art cannot ascertain how this feature can be achieved.

Regarding claim 47, it is not clear what a specific material (i.e. SiGe, SiC...) is being used to form the semiconductor capping layer that has a lattice constant larger than that of the bulk semiconductor body. Nowhere is this material recited in the disclosure. Without recitation of this material, one of ordinary skill in the art cannot ascertain how this feature can be achieved.

Regarding claim 48, it is not clear what a specific material (i.e. SiGe, SiC...) is being used to form the semiconductor capping layer that has a lattice constant smaller that that of the bulk semiconductor body. Nowhere is this material recited in the disclosure. Without recitation of this material, one of ordinary skill in the art cannot ascertain how this feature can be achieved.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 49-50 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 49 and 50 recite the limitation "strained semiconductor body" in line 2. There is insufficient antecedent basis for this limitation in the claim. "Strained semiconductor body" was not previously referred to in claim 44 from which claims 49 and 50 depend.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8, 10, 12-19 and 44-51 are rejected under 35 U.S.C. 103(c) as being unpatentable over Sugiyama et al. (US 2003/0227036) in view of Liu et al. (US 2004/0195624).

Regarding claims 1 and 51, Sugiyama et al. discloses in figure 2 a semiconductor device comprising a semiconductor (or strained semiconductor for claim 51) body 30 (para [0075], line 4) on a semiconductor substrate 10 (para [0075], line 3), said semiconductor body having a top surface and laterally opposite sidewalls; a semiconductor capping layer 40 (para [0075], line 6) formed on the top surface and on the sidewalls of said semiconductor body; a gate dielectric layer 70 (para [0076], line 3) formed on said semiconductor capping layer on said top surface and on said sidewalls of said semiconductor body; a gate electrode 80 (para [0076], line 1) having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and a pair of source/drain regions 50, 60 formed in said semiconductor body on opposite sides of said gate electrode. Note that element 40 is considered "capping layer" since it constitutes a similar structure and function as the claimed capping layer. Sugiyama et al. teaches a semiconductor body 30 on a SGOI substrate (para [0089], line1), not on a bulk semiconductor substrate. However, Liu et al. teaches in para [0003] a semiconductor body can be formed on a SGOI substrate or a bulk semiconductor substrate. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sugiyama et al. by having a semiconductor body on a bulk semiconductor substrate because SGOI substrate and a bulk semiconductor substrate are recognized in the art as equivalents.

Regarding claim 2, Sugiyama et al. discloses in figure 2 said capping layer 40 has a tensile stress. Applicant teaches, "a single crystalline silicon film formed on a silicon germanium alloy semiconductor body 208 will cause the single crystalline silicon film to have a tensile stress" (para [0017] of the instant application). Sugiyama teaches that the capping layer 40 is a silicon layer (para [0075]) formed on a silicon germanium alloy semiconductor body 30 (para [0075]). Therefore, the capping layer 40 inherently has a tensile stress.

Regarding claim 3, Sugiyama et al. discloses in figure 2 the semiconductor-capping layer has greater tensile stress on the sidewalls of the semiconductor body than on the top surface of the semiconductor body. Applicant teaches, "the silicon capping layer formed on the sidewalls 322 of the silicon germanium alloy will witness a substantial tensile stress and a lower but significant tensile strain on the top surface 319 of the silicon germanium alloy" (para [0043]). Sugiyama teaches that the capping layer 40 is a silicon layer (para [0075]) formed on a silicon germanium alloy semiconductor body 30 (para [0075]). Therefore, the semiconductor-capping layer inherently has greater tensile stress on the sidewalls of the semiconductor body than on the top surface of the semiconductor body.

Regarding claim 4, Sugiyama et al. discloses the source/drain regions are n type conductivity (para [0066]).

Regarding claim 5, Sugiyama et al. discloses the semiconductor substrate is a silicon substrate (para [0072], lines 5-6), wherein the semiconductor body is a silicon

germanium alloy (para [0075], line 4) and wherein the capping layer is a silicon film (para [0075]).

Regarding claim 6, applicant teaches in para [0017], "a single crystalline silicon capping layer 210 formed on a silicon carbon alloy semiconductor body 208 will cause the single crystalline silicon film 210 to have a compressive stress". Sugiyama et al. teaches the capping layer 40 is a silicon layer (para [0075]), lines 5-6) formed on a silicon germanium (SiGe) alloy semiconductor body 30 (para [0075], line 4), not on a silicon carbon (SiC) alloy body. However, Liu et al. teaches either SiGe or SiC can be alternatively used as an alloy body (para [0010]). Therefore, the combination of Sugiyama et al. and Liu et al. reads on claim 6.

Regarding claim 7, Sugiyama et al. and Liu et al together disclose the semiconductor-capping layer has a greater compressive stress on the sidewalls than on the top surface of the semiconductor body. Note that Sugiyama et al. and Liu et al. together disclose a silicon capping layer is formed on a silicon carbon body, and it is assumed that a silicon capping layer formed on a silicon carbon body inherently constitutes this feature.

Regarding claim 8, Sugiyama et al. discloses the semiconductor substrate is a silicon substrate (para [0089]), wherein the capping layer is a silicon film (para [0075]),l. and Liu et al. discloses in (para [0010]) the semiconductor body comprises a silicon carbon alloy.

Regarding claim 10, Sugiyama et al. discloses in figure 2 a semiconductor device comprising a silicon germanium body 30 (para [0075], line 4) on a silicon

monocrystalline substrate (para [0072], lines 5-6), said silicon germanium body having a top surface and laterally opposite sidewalls; a silicon film 40 (para [0075], line 6) formed on the top surface and on the sidewalls of said silicon germanium body; a gate dielectric layer 70 (para [0076], line 3) formed on said silicon film on said top surface of said silicon germanium body 30 and on said silicon film said sidewalls of said silicon germanium body; a gate electrode 80 (para [0076], line 1) having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and a pair of source/drain regions 50, 60 (para [0076], line 6) formed in said semiconductor body on opposite sides of said gate electrode. Sugiyama et al. teaches a silicon germanium body 30 on a SGOI substrate (para [0089], line1), not on a bulk silicon substrate. However, Liu et al. teaches in para [0003] a silicon germanium body can be formed on a SGOI substrate or a bulk silicon semiconductor substrate. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sugiyama et al. by having a silicon germanium body on a bulk silicon substrate because SGOI substrate and a bulk semiconductor substrate are recognized in the art as equivalents.

Regarding claim 12, Sugiyama et al. discloses the silicon film 40 has a thickness between 50-300A (para [0102], lines 6-7).

Regarding claim 13, Sugiyama et al. discloses the silicon germanium alloy comprises between 5-40% of germanium (para [0067], lines 1-3).

Regarding claim 14, Sugiyama et al. discloses the silicon germanium alloy comprises between 15-25% of germanium (para [0067], lines 1-3).

Regarding claim 15, Sugiyama et al. discloses the source/drain regions are n type conductivity (para [0066]).

Regarding claim 16, the difference between Sugiyama et al. and the claimed invention is a silicon carbon (SiC) alloy body (see rejection of claim 10 above). Note that Sugiyama et al. teaches a silicon germanium (SiGe) body. However, Liu et al. teaches in para [0010] either SiGe or SiC can be alternatively used as an alloy body. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sugiyama et al. by replacing SiGe body with SiC body because SiGe and SiC are recognized in the art as equivalents.

Regarding claims 17 and 18, Sugiyama et al. discloses the silicon film 40 has a thickness between 50-300A (para [0102], lines 6-7).

Regarding claim 19, Sugiyama et al. disclose the source/drain regions are p type (para [0077]). Note that Sugiyama teaches this structure can be manufactured for both p and n channel MISFET's (para [0077]).

Regarding claim 44, Sugiyama et al. discloses in figure 2 a semiconductor body 30 (para [0075], line 4) on a semiconductor substrate 10 (para [0075], line 3), said semiconductor body having a top surface and laterally opposite sidewalls, wherein said semiconductor body is comprised of a material (para [0075], line 4) which has a different lattice constant that said semiconductor substrate (para [0072], lines 5-6); a semiconductor capping layer 40 (para [0075], line 6) formed on the top surface on the sidewalls of said semiconductor body, wherein said semiconductor capping layer comprises a material which has a different lattice constant than said semiconductor

body; a gate dielectric 70 (para [0076], line 3) formed on said semiconductor capping layer on said top surface and on said sidewalls of said semiconductor body; a gate electrode 80 (para [0076], line 1) having a pair of laterally opposite sidewalls formed on and around said gate dielectric layer; and a pair of source/drain regions 50, 60 (para [0076], lines 6) formed in said semiconductor body on opposite sides of said gate electrode. Sugiyama et al. teaches a semiconductor body 30 on a SGOI substrate (para [0089], line1), not on a bulk semiconductor substrate. However, Liu et al. teaches in para [0003] a semiconductor body can be formed on a SGOI substrate or a bulk semiconductor substrate. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sugiyama et al. by having a semiconductor body on a bulk semiconductor substrate because SGOI substrate and a bulk semiconductor substrate are recognized in the art as equivalents.

Note that Sugiyama et al. teaches in (para [0075, line 4) the semiconductor body 30 is formed of SiGe, which has different lattice constant that the semiconductor substrate 10 formed of silicon (0072, lines 5-6). Further, the semiconductor-capping layer 40 is formed of silicon (para [0075], line 6), which has different lattice constant than the semiconductor body 30 formed of SiGe.

Regarding claim 45, it is assumed that the semiconductor body formed of SiGe (para [0075], line 4), which has a lattice constant larger than the lattice constant of the bulk semiconductor substrate formed of silicon (para [0003], line 8, Liu).

Regarding claim 46, it is assumed that the semiconductor body formed of SiC will have a lattice constant smaller than that of the bulk semiconductor substrate formed of silicon, and Liu et al. teaches. in para [0010] the semiconductor body is formed of SiC.

Regarding claim 47, it is assumed that the semiconductor-capping layer 40 formed of silicon (para [0075], lines 5-6, Sugiyama et al.) will have a lattice constant larger than that of the semiconductor body when the semiconductor body is formed of SiC, and Liu et al. teaches. in para [0010] the semiconductor body is formed of SiC.

Regarding claim 48, it is assumed that the semiconductor-capping layer 40 formed of silicon (para [0075], line 6), which has a lattice constant smaller than that of the semiconductor body formed of SiGe (para [0075], line 4).

Regarding claim 49, Sugiyama et al. and Liu et al. disclose the bulk semiconductor substrate is a silicon substrate (para [0003], line 8, Liu et al.), wherein said semiconductor body 30 is a silicon germanium (para [0075], line 4, Sugiyama et al.) and wherein the capping layer 40 is a silicon film (para [0075], lines 5-6).

Regarding claim 50, Sugiyama et al. and Liu et al. disclose the bulk semiconductor substrate is a silicon substrate (para [0003], line 8, Liu et al.) wherein said semiconductor body capping layer 40 is a silicon-capping layer (para [0075], lines 5-6, Sugiyama et al.), and the semiconductor body is formed of SiC (para [0010], Liu et al.).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiyama et al. and Liu et al. in view of figure 1A of the acknowledged prior art (APA).

Regarding claim 9, the difference between Sugiyama et al. and Liu et al. and the claimed invention is the semiconductor body comprising a silicon body. However, applicant disclosed in figure 1A of (APA) that the semiconductor body 102 is a silicon body. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sugiyama et al. and Liu et al. by having the semiconductor body comprising a silicon body to obtain a better lattice matching between the capping layer and the body since they are both formed of silicon.

Allowable Subject Matter

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 43 is allowed.

The following is a statement of reasons for the indication of allowable subject matter: The reference (s) of record do not teach or suggest, either singularly or in combination at least the limitation of "the silicon film formed thicker on the top surface of said silicon germanium body than on the sidewalls of said semiconductor body" for claim 43.

Response to Arguments

Applicant's arguments with respect to claims 1-19 and 44-51 have been considered but are moot in view of the new ground(s) of rejection.

Further, with respect to claims 6-8 and 16-19, applicant argues the Bohr reference and the Applicant's claimed invention were, at the time the invention was made, subject to an obligation of assignments to the same person, and that applicant respectfully requests removal of the 35 U.S.C 103 (a) rejection of claims 6-8 and 16-19 based on the Bohr reference. The Examiner agrees and has withdrawn the Bohr reference as an applied prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
September 20, 2005.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER